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U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.			Application No		
						M-10096 US			09/832,933		
VIENMATION DISCLOSURE STATEMENT BY APPLICANT						Applicant(s)					
(Use several sheets if necessary)						Lifeng Wu et al.					
SEP 1 2 2000 E						Filing Date			Group		
						April 11, 2001			2123		
TS TRAU	est.		U.S. P	atent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass		Filing Date If Appropriat			
TS	AA	5,533,197	Jul. 2, 1996	Moran et al.	1	(					
TS	AB	5,600,578	Feb. 4, 1997	Fang et al.							
TS	AC	5,606,518	Feb. 25, 1997	Fang et al.							
TS	AD	5,634,001	May 27, 1997	Mittl et al.							
TS	AE	5,974,247	Oct. 26, 1999	Yonezawa							
TS ·	AF	6,024,478	Feb. 15, 2000	Yamamoto							
TS	AG	6,047,247	Apr. 4, 2000	Iwanishi et al.							
TS	AH	6,278,964	Aug. 21, 2001	Fang et al.							
			Foreign	Patent Documents		i		t			
				<u> </u>				Trai	nslatio		
		Document	Date	Country	Class	Subc	ass	Yes	N		
									1		
	·	OTHER AR	T (Including Au	thor, Title, Date, Perti	nent Pages,	Etc.)					
TS	AI V/	Karam, Medhat, et al., "Implmentation of Hot-Carrier Reliability Simulation in Eldo" and related Internet material, Deep Submicron Technical Publication, dated September 2000.									
TS	AJ 🗸	Lou, Choon-Leong, et al., "A Novel Single-Device DC Method for Extraction of the Effective Mobility and Source-Drain Resistances of Fresh and Hot-Carrier Degraded Drain-Engineered MOSFET's", IEEE Transactions on Electron Devices, Vol. 45, No. 6, June 1998, pp. 1317-1323.									
TS	AK	Wong, H., et al., "Simulation of Hot-Carrier Reliability in MOS Integrated Circuits", PROC. 21 <sup>st</sup> International Conference on Microelectronics, Vol. 2, NIS, Yugoslavia, September 14-17, 1997, pp. 625-628.									
TS	AL	Hwang, Nam, et al., "Hot-Carrier Induced Series Resistance Enhancement Model (HISREM) of nMOSFET'S for Circuit Simulations and Reliability Projections", Microelectronics and Reliability, Vol. 35, No. 2, pp. 225-239, February 1995, pp. 225-239.									
TS	AM	Aur, S., et al., "Modeling of Hot Carrier Effects for LDD Mosfets", 1985 Symposium of VLSI Technology, pp. 112-113.									
TS	AN	Jang, Wenjie, et al., "Key Hot-Carrier Degradation Model Calibration and Verification Issues for Accurate AC Circuit-Level Reliability Simulation", IEEE, 1997, pp. 300-306.									
Examiner			Date Considered	d /Thomas Ster	vens/ (05	/25/20	06)				
				t citation is in conformation of this form with yo	ance with MP	EP 609; I	Draw lin				

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U.S. Department of Commerce, Patent and Trademark Office						et No.	Application No.				
						JS	09/832,933				
PROPRIATION DISCLOSURE STATEMENT BY APPLICANT						Applicant(s)					
(Use several sheets if necessary)						Lifeng Wu et al.					
SEP 1 2 20	12 E	Filing Date	Group 2123								
<u> </u>	<i>E</i> /	April 11, 2									
TEN'S TRAIN			U.S. Pa	tent Documents							
*Examiner Initial		ument nber	Date	Name	Class	Subclass	Filing Date If Appropriate				
			Foreign 1	Patent Documents		•					
		<u> </u>		<del></del>			Tran	slation			
	Doc	ument	Date	Country	Class	Subclass	Yes	No			
							<u> </u>				
		OTHER AR	T (Including Aut	hor, Title, Date, Pert	inent Pages, I	Etc.)					
TS		Hu, Chenming, "IC Reliability Simulation", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, March 1992, pp. 241-246.									
TS	AP Jian	Jiang, Wenjie, et al., "Assessing Circuit-Level Hot-Carrier Reliability", IEEE, 1998, pp. 173-179.									
TS		Ling, C.H., et al., "Simulation of Logarithmic Time Dependence of Hot Carrier Degradation in PMOSFETs", Semicond. Sci. Technol. 10, 1995, pp. 1659-1666.									
TS		Li, Chester C., et al., "A New Bi-directional PMOSFET Hot-Carrier Degradation Model for Circuit Reliability Simulation", IEEE, 1992, pp. 20.7.1-20.7.4.									
TS	Hot-	Quader, Khandker N., et al., "A Bidirectional NMOSFET Current Reduction Model for Simulation of Hot-Carrier-Induced Circuit Degradation", IEEE Transactions on Electron Devices, Vol. 40, No. 12, December 1993, pp. 2245-2254.									
26%		December 47723 pp. 2213 223 ii									
TS		A 1 40 110 01 1 11 100 11 0 14 14000 047 057									
TS	Ana	ylsis", Interna		SFET Hot Carrier Mo on VLSI Technology 287.							
Examiner			Date Considered		Stevens/	(05/25/20	06)				
				citation is in conform							

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